Omar Alhalawani

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Education

Bachelor of Engineering in Computer Systems Engineering — Ottawa, ON
Carleton University — CGPA: 11.6/12 (A+) — *Expected 2029*

- Ontario Professional Engineers Scholarship — Dean's Honour List

Technical Skills

Hardware & RTL: SystemVerilog (RTL), Verilog, synchronous digital design, FSMs, datapaths
Embedded & Low-Level: C, C++, Arduino, GPIO, SPI, I^2C, UART, ADC
Verification & Scripting: Python, Bash, simulation-based testing
Tools: Linux, Git, Vivado, Oscilloscope, Multimeter, Soldering

Experience

Embedded Hardware & Research Instrumentation Assistant — Sept. 2025 – Present
Carleton University – Engineering Laboratories — *Ottawa, ON*

- Designed and assembled custom electronic circuits through soldering and hardware integration for research instrumentation.
- Interfaced sensors, ADCs, and microcontrollers to support real-time experimental data collection.
- Developed low-level Arduino firmware for timing-critical control and data acquisition tasks.
- Debugged hardware and signal issues using oscilloscopes, multimeters, and systematic testing.

Teaching Assistant – Digital Systems (SYSC 2310) — Sept. 2025 – Present
Carleton University – Department of Systems & Computer Engineering — *Ottawa, ON*

- Supported students in digital logic, finite state machines, and synchronous circuit design.
- Assisted with debugging and validating HDL-based designs and timing-related issues.
- Reinforced verification habits through simulation, test cases, and incremental validation.

Hardware Repair Technician (Embedded & Board-Level) — July 2022 – Sept. 2023
uBreakiFix — *Ottawa, ON*

- Performed component-level diagnostics and repair on consumer electronic and embedded systems.
- Diagnosed power, signal integrity, and board-level faults using systematic testing methods.
- Worked with microcontrollers, peripherals, and low-level hardware interfaces during device repair.
- Developed disciplined debugging workflows under time and reliability constraints.

Projects

Synchronous FIFO RTL Design & Verification — *SystemVerilog*

- Designed a synthesizable synchronous FIFO with parameterized depth and data width.
- Implemented read/write pointer logic, full/empty status flags, and valid/ready handshaking.
- Developed a self-checking SystemVerilog testbench with directed and corner-case tests.

FPGA-Based Arithmetic Display System — *Verilog, Vivado*

- Designed a synchronous digital system integrating arithmetic, control, and display logic on FPGA.
- Implemented a datapath with add/subtract functionality and multiplexed input selection.
- Designed an FSM-based control unit to manage input capture, operation selection, and output display.
- Developed combinational decoding logic to drive a 7-segment display with registered outputs.
- Verified functionality through simulation and debugged timing and logic issues during FPGA bring-up.

EMG Signal Acquisition & Processing System — *Arduino, Python*

- Designed an EMG data acquisition and signal conditioning pipeline using MyoWare sensors and microcontrollers.

Extracurricular Involvement

Carleton Planetary Robotics Team (FPGA Subteam) — *2025 – Present*

- Developing FPGA logic for rover subsystems used in competitive robotics environments.

Biomedical Carleton Applied Research and Engineering (BioCARE) — *2025 – Present*

- Applying hardware and software skills to support biomedical research projects.